2811

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **HORIGUCHI, Naoto et al.**

Serial No.: **09/726,386**

Filed: **December 1, 2000**

Group Art Unit: **2811**

Examiner: **Tran, Thien F**

9/a
FJones
10-30-02

FOR: **SEMICONDUCTOR MEMORY WITH FLOATING GATE TYPE FET**

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

July 10, 2002

Sir:

In response to the Office Action dated **April 10, 2002**, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claim 1 to read as follows:

1. (Amended) A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a direct tunneling phenomenon;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by the